32. (amended) A capacitor construction comprising a first capacitor electrode over a substrate, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first and second electrodes.

33. (amended) The construction of claim 32 wherein the barrier layer has a thickness of less than about 12 Angstroms.

B1

34. (amended) The construction of claim 32 wherein the barrier layer comprises Al_2O_3.

35. (amended) The construction of claim 32 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

sub C1

36. (amended) A capacitor construction comprising:

a first capacitor electrode over a substrate;

an insulative barrier layer to oxygen diffusion over the first electrode, the barrier layer comprising a chemisorption product of first and second precursor layers;

a capacitor dielectric layer over the first electrode; and

a second capacitor electrode over the dielectric layer and the barrier layer.

37. (amended) The construction of claim 36 wherein the barrier layer has a thickness of less than about 12 Angstroms.

B1 cont'd

38. (amended) The construction of claim 36 wherein the barrier layer comprises Al_2O_3.

39. (amended) The construction of claim 36 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

40. (new) A memory array comprising:

a plurality of capacitor constructions each having a first capacitor electrode over a substrate, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first and second electrodes.

B2

41. (new) The array of claim 40 wherein the barrier layer has a thickness of less than about 12 Angstroms.

42. (new) The array of claim 40 wherein the barrier layer comprises Al_2O_3.

43. (new) The array of claim 40 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

Sub D2

44. (new) The array of claim 40 ~~wherein the~~ barrier layer comprises a chemisorption product of first and second precursor layers.

45. (new) A plurality of memory dice, each die comprising:

a section of a monocrystalline semiconductor wafer; and

a capacitor construction comprising a first capacitor electrode over the wafer, a capacitor dielectric layer over the first electrode, a second capacitor electrode over the dielectric layer, and an atomic layer deposited insulative barrier layer to oxygen diffusion between the first and second electrodes.

B2 cont'd

46. (new) The dice of claim 45 wherein the barrier layer has a thickness of less than about 12 Angstroms.

47. (new) The dice of claim 45 wherein the barrier layer comprises Al_2O_3.

48. (new) The dice of claim 45 wherein the barrier layer exhibits a K factor of greater than about 7 at 20° C.

Sub D3

49. (new) The ~~dice~~ of claim 45 wherein the barrier layer comprises a chemisorption product of first and second precursor layers.